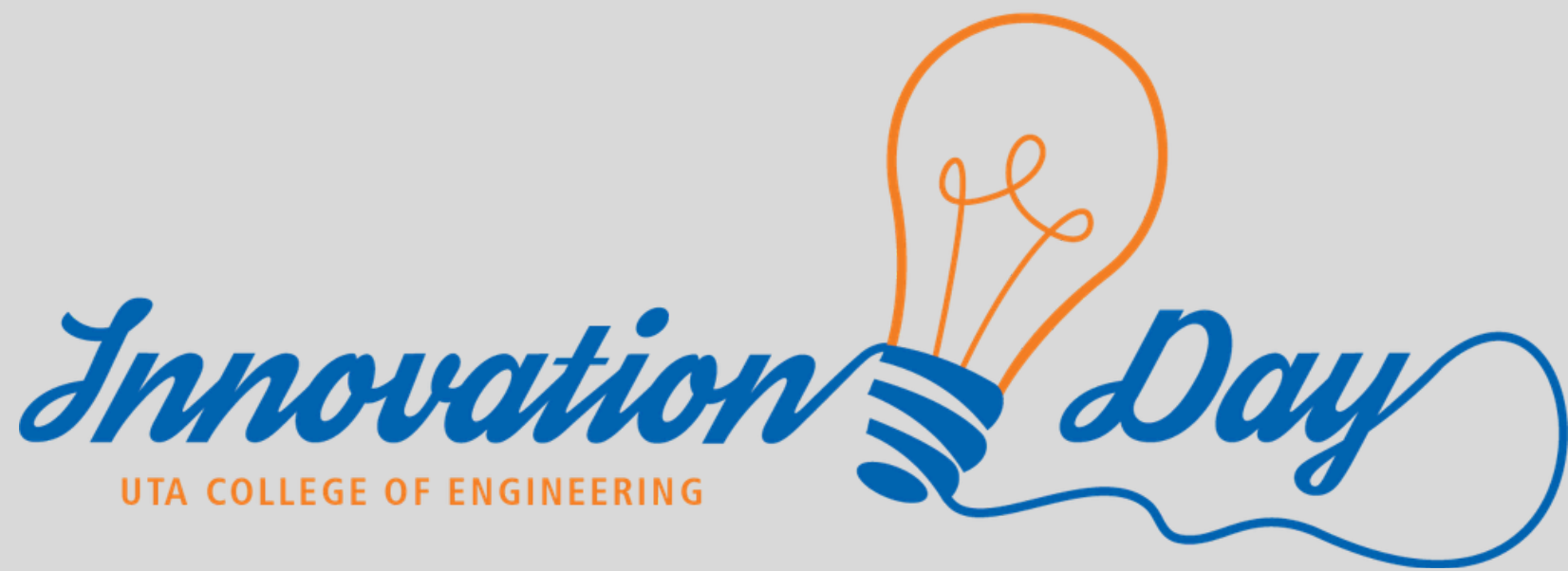


3D Crossbar Simulator

REU PROJECT

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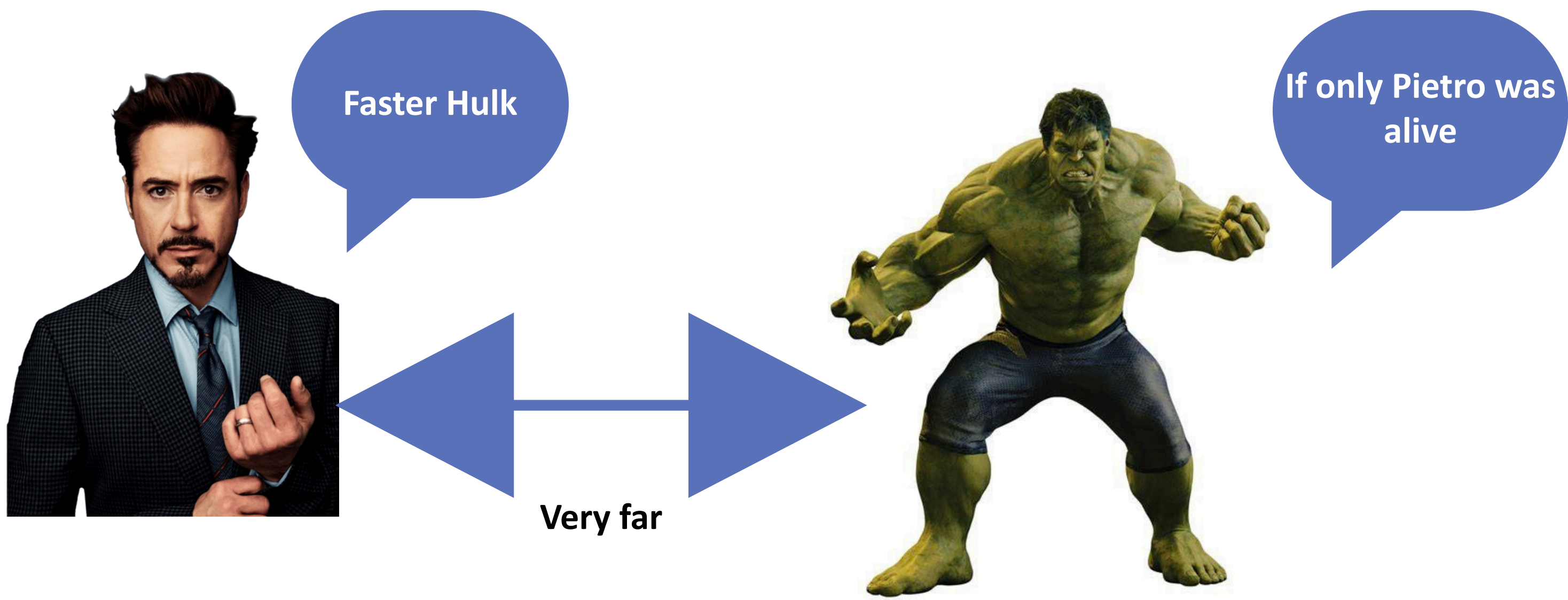


Executive Summary

This work presents a simulator for a 3D memristive crossbar architecture, extending conventional 2D in-memory computing systems into the third dimension. By stacking multiple 2D crossbars and introducing vertical memristive interconnects, the proposed design enables computation along the x, y, and z axes, significantly increasing computational density and parallelism. The simulator models both ideal circuit behavior and key hardware non-idealities, providing a flexible and realistic platform for analyzing next-generation in-memory computing architectures.

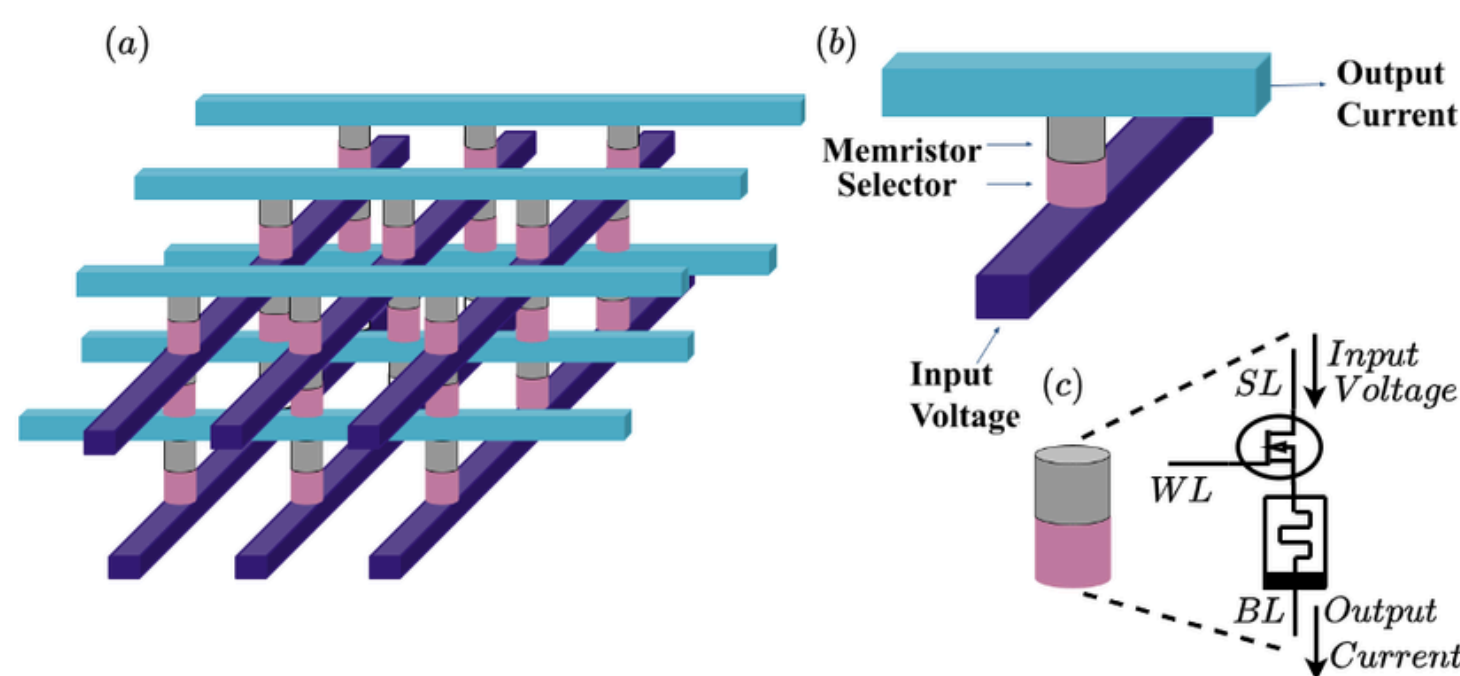
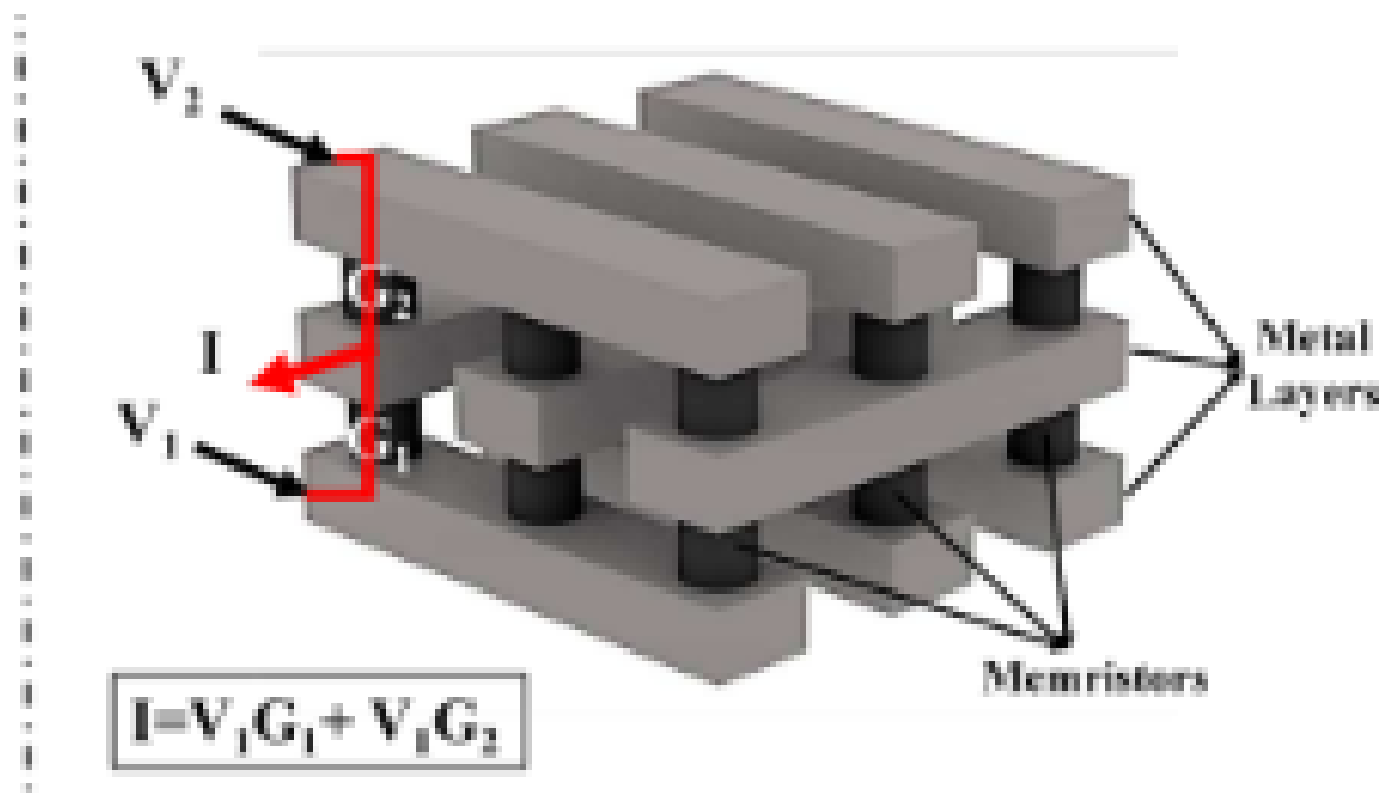
Background

Traditional computing systems are fundamentally limited by the von Neumann bottleneck, where data must continuously move between memory and the processor. This data movement dominates latency and energy consumption, especially in workloads such as machine learning.



A useful analogy is to imagine the Incredible Hulk extracting raw minerals in a cave, while Tony Stark processes them in Stark Tower across New York. Hulk is extremely strong and Stark is highly intelligent, but the constant transportation of materials slows down the entire process. In-memory computing is equivalent to placing a capable scientist alongside Hulk, partially processing the minerals before sending them to Stark, thereby reducing the delay and improving overall efficiency.

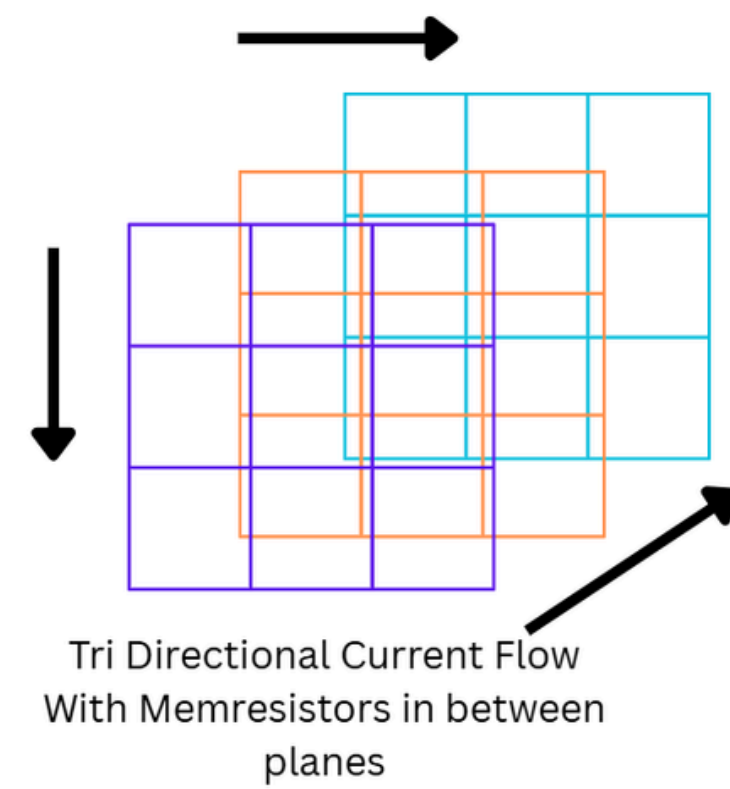
Memristive 2D crossbar arrays address this issue by performing computation directly where data is stored, particularly enabling efficient matrix-vector multiplications using Ohm's Law and Kirchhoff's laws. This area is well-established, with simulators such as CrossSim demonstrating accurate modeling of analog in-memory computing systems. However, 2D crossbars remain constrained in area and scalability. Extending these architectures into 3D offers a path toward significantly higher computational throughput without increasing planar footprint.



Technical Design

The proposed architecture is constructed by stacking p layers of traditional 2D crossbars, each of dimension m × n. Unlike simplified models, each memristive element is represented using two nodes, one corresponding to the wordline connection and the other to the bitline connection, enabling more precise circuit modeling.

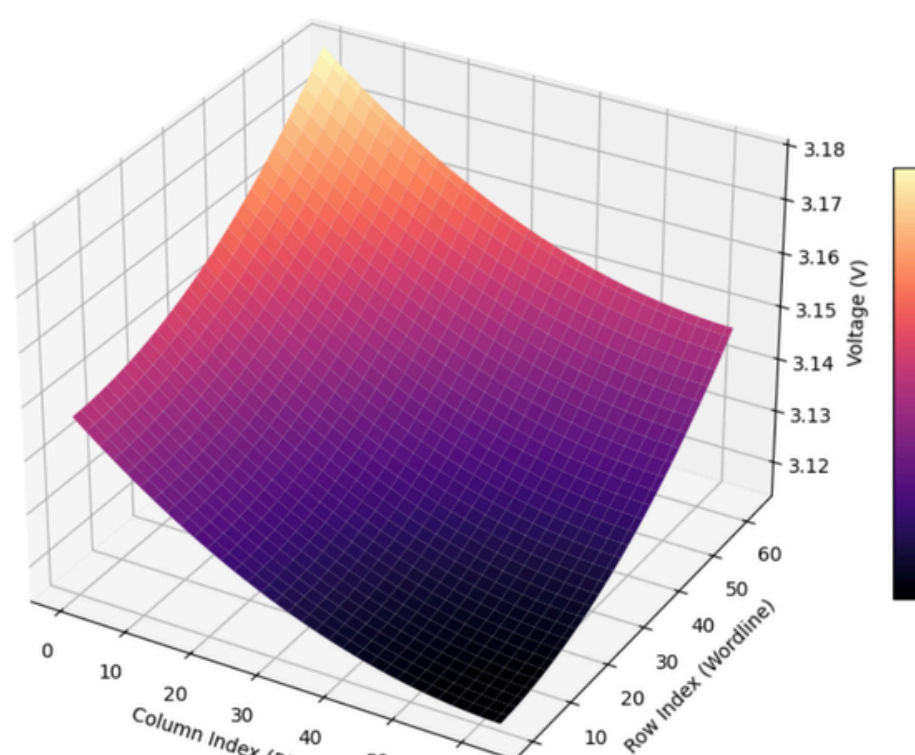
To extend computation into the third dimension, corresponding nodes in adjacent layers are connected using memristors along the z-axis. This introduces vertical current paths and allows interactions between layers. For a system with p crossbars, the total number of vertical memristive connections is given by 2(p-1)mn. This results in a fully interconnected 3D resistive network, where current can propagate and contribute to computation across all three spatial dimensions, rather than being restricted to planar operations.



Technical Implementation

The simulator models the full circuit behavior using Kirchhoff's Current Law (KCL) and Kirchhoff's Voltage Law (KVL), forming a system of linear equations that describe the network. Due to the scale of the architecture, these equations are represented using a sparse matrix formulation, enabling efficient numerical solving. To ensure realism, the simulator incorporates key non-idealities observed in physical memristive systems. These include parasitic resistances in interconnects, IR voltage drops across long lines, and conductance drift in memristive devices over time. These effects are critical for accurately evaluating large-scale crossbar behavior.

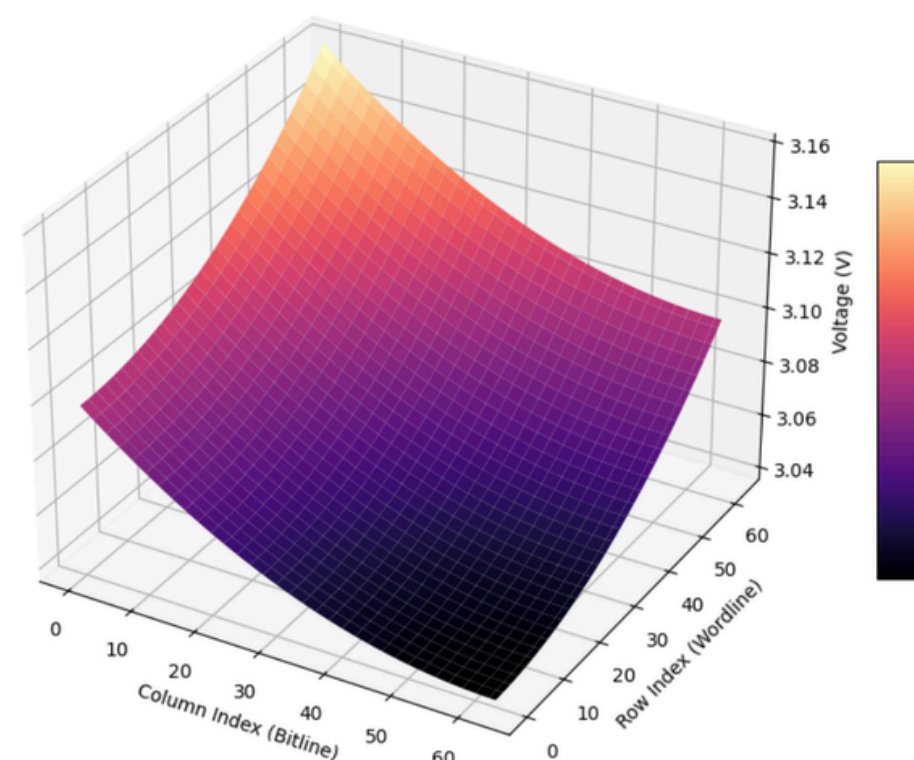
Sneak Path & IR Drop Analysis: Voltage Drop Across Target Cells



Average Case IR Drop for 2D Crossbars

The framework is designed to be highly configurable at the circuit level. Memristors can be dynamically set between low-resistance (LRS) and high-resistance (HRS) states, allowing different weight configurations. The architecture supports two independent input voltage matrices applied along adjacent faces of the 3D structure, sharing a common edge, enabling multi-directional stimulation. Additionally, a configurable output voltage matrix is used to define biasing conditions and measurement schemes at the terminals.

Sneak Path & IR Drop Analysis: Voltage Drop Across Target Cells



Worst Case IR Drop for 2D Crossbars

Conclusion

By extending traditional 2D crossbar arrays into a 3D memristive architecture, this work demonstrates a pathway toward significantly improved computational density and parallelism in in-memory computing systems. The proposed simulator provides a scalable and realistic modeling framework, capturing both ideal functionality and critical hardware non-idealities. This enables meaningful evaluation of future architectures designed to mitigate the von Neumann bottleneck and support increasingly data-intensive applications.

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